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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	664	(712/245).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 18:28
L2	62	1 and (out adj order$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 18:28
L3	0	((instruction adj queue$3) with (rename$5 reorder$5)) and 2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 18:28
L4	39	((instruction adj queue$3) (rename$5 reorder$5)) and 2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 18:28
S1	2	("20010042192").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 18:25
S4	5	"6308260"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 14:04
S5	484	(712/215).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 14:03
S6	471	(712/216).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 14:04

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S7	521	(712/217).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 14:04
S8	186	(rename$5 reorder$5) and S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 14:05
S9	231	(rename$5 reorder$5) and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 14:05
S10	325	(rename$5 reorder$5) and S7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 14:05
S11	9	((instruction adj queue$3) with (rename$5 reorder$5)) and S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 14:05
S12	16	((instruction adj queue$3) with (rename$5 reorder$5)) and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 18:28
S13	16	((instruction adj queue$3) with (rename$5 reorder$5)) and S7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/06 14:05

Published before September 1998
Terms used **instruction issue rename register out of order**

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1 SIMP (Single Instruction stream/Multiple instruction Pipelining): a novel high-speed single-processor architecture
K. Murakami, N. Irie, S. Tomita
April 1989 **ACM SIGARCH Computer Architecture News , Proceedings of the 16th annual international symposium on Computer architecture ISCA '89**, Volume 17 Issue 3
Publisher: ACM Press
Full text available: pdf(1.23 MB) Additional Information: full citation, abstract, references, citings, index terms

SIMP is a novel multiple instruction-pipeline parallel architecture. It is targeted for enhancing the performance of SISD processors drastically by exploiting both temporal and spatial parallelisms, and for keeping program compatibility as well. Degree of performance enhancement achieved by SIMP depends on; i) how to supply multiple instructions continuously, and ii) how to resolve data and control dependencies effectively. We have devised the outstanding techniques for instruction fetch an ...

2 Facilitating superscalar processing via a combined static/dynamic register renaming scheme
Eric Sprangle, Yale Patt
November 1994 **Proceedings of the 27th annual international symposium on Microarchitecture**
Publisher: ACM Press
Full text available: pdf(544.45 KB) Additional Information: full citation, references, citings, index terms

Keywords: out-of-order execution, predicated execution, register renaming, superscalar processors

3 Instruction-level parallelism from execution interlock collapsing
Nadeem Malik, Richard J. Eickemeyer, Stamatis Vassiliadis
September 1992 **ACM SIGARCH Computer Architecture News**, Volume 20 Issue 4
Publisher: ACM Press
Full text available: pdf(579.86 KB) Additional Information: full citation, abstract, citings, index terms

An innovative technique has been developed that permits the collapsing of execution interlocks between integer ALU operations as well as between address generation operations, allowing parallel execution of two instructions, having true dependencies, in a single cycle. Given that the proposed scheme has been shown not to increase the machine cycle time, it potentially provides an attractive means for increasing the

instruction--level parallelism. Preliminary results show that within the basic bl ...

4 Interlock collapsing ALU for increased instruction-level parallelism

Nadeem Malik, Richard J. Eickemeyer, Stamatis Vassiliadis

December 1992 **ACM SIGMICRO Newsletter , Proceedings of the 25th annual international symposium on Microarchitecture MICRO 25**, Volume 23 Issue 1-2

Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(1.12 MB) Additional Information: full citation, references, citings, index terms

5 Limitation of superscalar microprocessor performance

Thang Tran, Chuan-lin Wu

December 1992 **ACM SIGMICRO Newsletter , Proceedings of the 25th annual international symposium on Microarchitecture MICRO 25**, Volume 23 Issue 1-2

Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(495.55 KB) Additional Information: full citation, references, citings, index terms

6 Tuning compiler optimizations for simultaneous multithreading

Jack L. Lo, Susan J. Eggers, Henry M. Levy, Sujay S. Parekh, Dean M. Tullsen

December 1997 **Proceedings of the 30th annual ACM/IEEE international symposium on Microarchitecture**

Publisher: IEEE Computer Society

Full text available: pdf(1.45 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Compiler optimizations are often driven by specific assumptions about the underlying architecture and implementation of the target machine. For example, when targeting shared-memory multiprocessors, parallel programs are compiled to minimize sharing, in order to decrease high-cost, inter-processor communication. This paper reexamines several compiler optimizations in the context of simultaneous multithreading (SMT), a processor architecture that issues instructions from multiple threads to the f ...

Keywords: cache size, compiler optimizations, cyclic algorithm, fine-grained sharing, instructions, inter-processor communication, inter-thread instruction-level parallelism, latency hiding, loop tiling, loop-iteration scheduling, memory system resources, optimising compilers, parallel architecture, parallel programs, performance, processor architecture, shared-memory multiprocessors, simultaneous multithreading, software speculative execution

7 Converting thread-level parallelism to instruction-level parallelism via simultaneous multithreading

Jack L. Lo, Joel S. Emer, Henry M. Levy, Rebecca L. Stamm, Dean M. Tullsen, S. J. Eggers

August 1997 **ACM Transactions on Computer Systems (TOCS)**, Volume 15 Issue 3

Publisher: ACM Press

Full text available: pdf(526.39 KB) Additional Information: full citation, abstract, references, citings, index terms, review

To achieve high performance, contemporary computer systems rely on two forms of parallelism: instruction-level parallelism (ILP) and thread-level parallelism (TLP). Wide-issue super-scalar processors exploit ILP by executing multiple instructions from a single program in a single cycle. Multiprocessors (MP) exploit TLP by executing different threads in parallel on different processors. Unfortunately, both parallel processing styles statically partition processor resources, thus preventing t ...

Keywords: cache interference, instruction-level parallelism, multiprocessors,

multithreading, simultaneous multithreading, thread-level parallelism

8 Enhanced superscalar hardware: the schedule table

J. K. Pickett, D. G. Meyer

December 1993 **Proceedings of the 1993 ACM/IEEE conference on Supercomputing**

Publisher: ACM Press

Full text available: pdf(886.54 KB) Additional Information: full citation, references, index terms

9 The case for a single-chip multiprocessor

Kunle Olukotun, Basem A. Nayfeh, Lance Hammond, Ken Wilson, Kunyung Chang

September 1996 **ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proceedings of the seventh international conference on Architectural support for programming languages and operating systems ASPLOS-VII**, Volume 31 , 30 Issue 9 , 5

Publisher: ACM Press

Full text available: pdf(1.10 MB) Additional Information: full citation, abstract, references, citings, index terms

Advances in IC processing allow for more microprocessor design options. The increasing gate density and cost of wires in advanced integrated circuit technologies require that we look for new ways to use their capabilities effectively. This paper shows that in advanced technologies it is possible to implement a single-chip multiprocessor in the same area as a wide issue superscalar processor. We find that for applications with little parallelism the performance of the two microarchitectures is co ...

10 OHMEGA: a VLSI superscalar processor architecture for numerical applications

Masaitsu Nakajima, Hiraku Nakano, Yasuhiro Nakakura, Tadahiro Yoshida, Yoshiyuki Goi, Yuji Nakai, Reiji Segawa, Takeshi Kishida, Hiroshi Kadota

April 1991 **ACM SIGARCH Computer Architecture News , Proceedings of the 18th annual international symposium on Computer architecture ISCA '91**, Volume 19 Issue 3

Publisher: ACM Press

Full text available: pdf(941.13 KB) Additional Information: full citation, references, citings, index terms

11 Initial results on the performance and cost of vector microprocessors

Corinna G. Lee, Derek J. DeVries

December 1997 **Proceedings of the 30th annual ACM/IEEE international symposium on Microarchitecture**

Publisher: IEEE Computer Society

Full text available: pdf(1.73 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Increasingly wider superscalar processors are experiencing diminishing performance returns while requiring larger portions of die area dedicated to control rather than datapath. As an alternative to using these processors to exploit parallelism effectively, we are investigating the viability of using single-chip vector microprocessors. This paper presents some initial results of our investigation where we compare the performance and cost of vector microprocessors to that of aggressive, out-of-or ...

12 Exploiting instruction level parallelism in processors by caching scheduled groups

Ravi Nair, Martin E. Hopkins

May 1997 **ACM SIGARCH Computer Architecture News , Proceedings of the 24th annual international symposium on Computer architecture ISCA '97**, Volume 25 Issue 2

Publisher: ACM Press

Full text available: pdf(2.01 MB) Additional Information: full citation, abstract, references, citings, index terms

Modern processors employ a large amount of hardware to dynamically detect parallelism in single-threaded programs and maintain the sequential semantics implied by these programs. The complexity of some of this hardware diminishes the gains due to parallelism because of longer clock period or increased pipeline latency of the machine.In this paper we propose a processor implementation which dynamically schedules groups of instructions while executing them on a fast simple engine and caches them f ...

13 A comparison of three current superscalar designs

Michael Laird

June 1992 **ACM SIGARCH Computer Architecture News**, Volume 20 Issue 3

Publisher: ACM Press

Full text available: pdf(824.41 KB) Additional Information: full citation, abstract, index terms

A standardized view of superscalar architectures is presented, and three current superscalar designs are comparedusing this framework. The designs studied are the Metaflow Light-ning SPARC, the IBM RS/6000, and the Intel i960MM.

14 Performance evaluation of the PowerPC 620 microarchitecture

Trung A. Diep, Christopher Nelson, John Paul Shen

May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture ISCA '95**, Volume 23 Issue 2

Publisher: ACM Press

Full text available: pdf(1.35 MB) Additional Information: full citation, abstract, references, citings, index terms

The PowerPC 620™ microprocessor is the most recent and performance leading member of the PowerPC™ family. The 64-bit PowerPC 620 microprocessor employs a two-phase branch prediction scheme, dynamic renaming for all the register files, distributed multi-entry reservation stations, true out-of-order execution by six execution units, and a completion buffer for ensuring precise exceptions. This paper presents an instruction-level performance evaluation of the 620 microarchitectu ...

15 Improving superscalar instruction dispatch and issue by exploiting dynamic code sequences

Sriram Vajapeyam, Tulika Mitra

May 1997 **ACM SIGARCH Computer Architecture News , Proceedings of the 24th annual international symposium on Computer architecture ISCA '97**, Volume 25 Issue 2

Publisher: ACM Press

Full text available: pdf(1.76 MB) Additional Information: full citation, abstract, references, citings, index terms

Superscalar processors currently have the potential to fetch multiple basic blocks per cycle by employing one of several recently proposed instruction fetch mechanisms. However, this increased fetch bandwidth cannot be exploited unless pipeline stages further downstream correspondingly improve. In particular, register renaming a large number of instructions per cycle is difficult. A large instruction window, needed to receive multiple basic blocks per cycle, will slow down dependence resolution ...

16 Exploiting choice: instruction fetch and issue on an implementable simultaneous multithreading processor

Dean M. Tullsen, Susan J. Eggers, Joel S. Emer, Henry M. Levy, Jack L. Lo, Rebecca L. Stamm

May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture ISCA '96**, Volume 24 Issue 2

Publisher: ACM Press

Full text available: pdf(1.48 MB) Additional Information: full citation, abstract, references, citings, index terms

Simultaneous multithreading is a technique that permits multiple independent threads to issue multiple instructions each cycle. In previous work we demonstrated the performance potential of simultaneous multithreading, based on a somewhat idealized model. In this paper we show that the throughput gains from simultaneous multithreading can be achieved *without* extensive changes to a conventional wide-issue superscalar, either in hardware structures or sizes. We present an architecture for s ...

17 Implementation trade-offs in using a restricted data flow architecture in a high performance RISC microprocessor

M. Simone, A. Essen, A. Ike, A. Krishnamoorthy, T. Maruyama, N. Patkar, M. Ramaswami, M. Shebanow, V. Thirumalaiswamy, D. Tovey

May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture ISCA '95**, Volume 23 Issue 2

Publisher: ACM Press

Full text available: pdf(1.04 MB) Additional Information: full citation, abstract, references, citings, index terms

The implementation of a superscalar, speculative execution SPARC-V9 microprocessor incorporating Restricted Data Flow principles required many design trade-offs. Consideration was given to both performance and cost. Performance is largely a function of cycle time and instructions executed per cycle while cost is primarily a function of die area. Here we describe our Restricted Data Flow implementation and the means with which we arrived at its configuration. Future semiconductor technology advan ...

18 Complexity-effective superscalar processors

Subbarao Palacharla, Norman P. Jouppi, J. E. Smith

May 1997 **ACM SIGARCH Computer Architecture News , Proceedings of the 24th annual international symposium on Computer architecture ISCA '97**, Volume 25 Issue 2

Publisher: ACM Press

Full text available: pdf(2.21 MB) Additional Information: full citation, abstract, references, citings, index terms

The performance tradeoff between hardware complexity and clock speed is studied. First, a generic superscalar pipeline is defined. Then the specific areas of register renaming, instruction window wakeup and selection logic, and operand bypassing are analyzed. Each is modeled and Spice simulated for feature sizes of 0.8µm, 0.35µm, and 0.18µm. Performance results and trends are expressed in terms of issue width and window size. Our analysis indicates that window wakeu ...

19 The expandable split window paradigm for exploiting fine-grain parallelsim

Manoj Franklin, Gurindar S. Sohi

April 1992 **ACM SIGARCH Computer Architecture News , Proceedings of the 19th annual international symposium on Computer architecture ISCA '92**, Volume 20 Issue 2

Publisher: ACM Press

Full text available: pdf(1.25 MB) Additional Information: full citation, abstract, references, citings, index terms

We propose a new processing paradigm, called the Expandable Split Window (ESW) paradigm, for exploiting fine-grain parallelism. This paradigm considers a window of instructions (possibly having dependencies) as a single unit, and exploits fine-grain parallelism by overlapping the execution of multiple windows. The basic idea is to connect multiple sequential processors, in a decoupled and decentralized manner, to achieve overall multiple issue. This processing paradigm shares a number of pr ...

20 RISC versus CISC: a tale of two chips

Dileep Bhandarkar

March 1997 **ACM SIGARCH Computer Architecture News**, Volume 25 Issue 1
Publisher: ACM Press
Full text available: pdf(771.63 KB) Additional Information: full citation, abstract, index terms

This paper compares an aggressive RISC and CISC implementation built with comparable technology. The two chips are the Alpha* 21164 and the Intel Pentium® Pro processor. The paper presents performance comparisons for industry standard benchmarks and uses performance counter statistics to compare various aspects of both designs.

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Published before September 1998
Terms used **instruction issue rename register out of order instruction queue**

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1 Converting thread-level parallelism to instruction-level parallelism via simultaneous multithreading

Jack L. Lo, Joel S. Emer, Henry M. Levy, Rebecca L. Stamm, Dean M. Tullsen, S. J. Eggers
August 1997 **ACM Transactions on Computer Systems (TOCS)**, Volume 15 Issue 3
Publisher: ACM Press

Full text available: pdf(526.39 KB) Additional Information: full citation, abstract, references, citings, index terms, review

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Kunle Olukotun, Basem A. Nayfeh, Lance Hammond, Ken Wilson, Kunyung Chang
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Publisher: ACM Press

Full text available: pdf(1.10 MB) Additional Information: full citation, abstract, references, citings, index terms

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3 Exploiting choice: instruction fetch and issue on an implementable simultaneous multithreading processor

Dean M. Tullsen, Susan J. Eggers, Joel S. Emer, Henry M. Levy, Jack L. Lo, Rebecca L. Stamm

May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture ISCA '96**, Volume 24 Issue 2
Publisher: ACM Press

Full text available: pdf(1.48 MB) Additional Information: full citation, abstract, references, citings, index terms

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Jack L. Lo, Susan J. Eggers, Henry M. Levy, Sujay S. Parekh, Dean M. Tullsen
December 1997 **Proceedings of the 30th annual ACM/IEEE international symposium on Microarchitecture**
Publisher: IEEE Computer Society

Full text available: pdf(1.45 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

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Keywords: cache size, compiler optimizations, cyclic algorithm, fine-grained sharing, instructions, inter-processor communication, inter-thread instruction-level parallelism, latency hiding, loop tiling, loop-iteration scheduling, memory system resources, optimising compilers, parallel architecture, parallel programs, performance, processor architecture, shared-memory multiprocessors, simultaneous multithreading, software speculative execution

5 Improving superscalar instruction dispatch and issue by exploiting dynamic code sequences
Sriram Vajapeyam, Tulika Mitra
May 1997 **ACM SIGARCH Computer Architecture News , Proceedings of the 24th annual international symposium on Computer architecture ISCA '97**, Volume 25 Issue 2
Publisher: ACM Press

Full text available: pdf(1.76 MB) Additional Information: full citation, abstract, references, citings, index terms

Superscalar processors currently have the potential to fetch multiple basic blocks per cycle by employing one of several recently proposed instruction fetch mechanisms. However, this increased fetch bandwidth cannot be exploited unless pipeline stages further downstream correspondingly improve. In particular, register renaming a large number of instructions per cycle is difficult. A large instruction window, needed to receive multiple basic blocks per cycle, will slow down dependence resolution ...

6 Limitation of superscalar microprocessor performance
Thang Tran, Chuan-lin Wu
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Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(495.55 KB) Additional Information: full citation, references, citings, index terms

7 An analysis of database workload performance on simultaneous multithreaded processors

Jack L. Lo, Luiz André Barroso, Susan J. Eggers, Kourosh Gharachorloo, Henry M. Levy, Sujay S. Parekh

April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture ISCA '98**, Volume 26 Issue 3

Publisher: IEEE Computer Society, ACM Press

Full text available: pdf(1.57 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Simultaneous multithreading (SMT) is an architectural technique in which the processor issues multiple instructions from multiple threads each cycle. While SMT has been shown to be effective on scientific workloads, its performance on database systems is still an open question. In particular, database systems have poor cache performance, and the addition of multithreading has the potential to exacerbate cache conflicts.This paper examines database performance on SMT processors using traces of th ...

8 Dynamic instruction reuse

Avinash Sodani, Gurindar S. Sohi

May 1997 **ACM SIGARCH Computer Architecture News , Proceedings of the 24th annual international symposium on Computer architecture ISCA '97**, Volume 25 Issue 2

Publisher: ACM Press

Full text available: pdf(1.97 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper introduces the concept of dynamic instruction reuse. Empirical observations suggest that many instructions, and groups of instructions, having the same inputs, are executed dynamically. Such instructions do not have to be executed repeatedly --- their results can be obtained from a buffer where they were saved previously. This paper presents three hardware schemes for exploiting the phenomenon of dynamic instruction reuse, and evaluates their effectiveness using execution-driven simul ...

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Williams, T.; Patkar, N.; Shen, G.;
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Grunbacher, H.;
Frontiers in Education Conference, 1998. FIE '98. 28th Annual
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Computer Architecture, 1998. Proceedings. The 25th Annual International Symposium on
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Shen, G.; Patkar, N.; Ando, H.; Chang, D.; Chen, C.; Chien Chen; Chen, F.; Forssell, P.; Gmuender, J.; Kitahara, T.; Hungwen Li; Lyon, D.; Montoye, R.; Peng, L.; Savkar, S.; Sherred, J.; Simone, M.; Swami, R.; Tovey, D.; Williams, T.;
Solid-State Circuits Conference, 1995. Digest of Technical Papers. 42nd ISSCC, 1995 IEEE International
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8. **A novel renaming scheme to exploit value temporal locality through physical register reuse and unification**
Jourdan, S.; Ronen, R.; Bekerman, M.; Shomar, B.; Yoaz, A.;
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Web Results **1** - **9** of about **17** for **"out of order" "issuing instruction" "rename register"** . (**1.25** seconds)

Citations: The Metaflow Architecture - Popescu, Schultz, Spracklen ...
... may be used by a currently **issuing instruction** without waiting for it to be ... Metaflow s DRIS The Metaflow architecture [8] implements **out of order** ...
citeseer.ist.psu.edu/context/629790/0 - 21k - Cached - Similar pages

esp@cenet description view
If the processor is to fully support **out-of-order** execution, each of the result registers must be allocated a **rename register** in the cycle when a complex ...
v3.espacenet.com/ textdes?IDX=EP1256053&QPN=EP1256053 - 53k - Cached - Similar pages

Superscalar risc instruction scheduling - Patent 5737624
A register renaming system for **out-of-order** execution of a set of ... 102 are ready for **issuing. Instruction** decode logic (not shown) indicates to Issuer ...
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Superscalar RISC instruction scheduling - US Patent 6289433
when instructions are Issued **out of order** and complete **out of order**, ... the present INVENTION does not actually **Rename register** addresses. ...
www.patentstorm.us/patents/6289433.html - 89k - Supplemental Result - Cached - Similar pages

Method and circuit for using a single rename array in a ...
a single **rename register** array is used in an SMT processor. ... thread identification bit TB 236, from the **issuing instruction**, is coupled as signal 226 to ...
www.freshpatents.com/ Method-and-circuit-for-using-a-single-rename-array-in-a-simultaneous-multithread-sys... - 46k - Supplemental Result - Cached - Similar pages

[PS] SPARC64-III User's Guide HAL Computer Systems, Inc. Campbell ...
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Some **out-of-order** execution is allowed, but some operations must execute in order. ... Unlike Serial number and **rename register**, the DFM queue entry becomes ...
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[PDF] chap04.new new
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When an instruction issues, it is allocated a **rename register**; ... pipelines that specify the destination in the **issuing instruction** and in which an is- ...
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[PDF] chap04.new new
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Page 1. 4 "Who's first?" "America." "Who's second?" "Sir, there is no second." Dialog between two observers of ...
www.whatever.org.ar/. ../chap04.pdf - Supplemental Result - Similar pages

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must be the first or last slot of the current **issuing instruction** window. ... Unlike Serial number and **rename register**, the DFM queue entry becomes ...
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"out of order" "issuing instruction" "re Search

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Web Results **1 - 10** of about **156** for **"issue instruction "rename register" "instruction queue"**. (**0.47** seconds)

POWER4 System Microarchitecture -- Page 3
Group Dispatch and **Instruction Issue: Instruction** groups are dispatched into the issue ... **Rename Register**: For each **register** that is renamed and set by an ...
www-1.ibm.com/servers/eserver/ pseries/hardware/whitepapers/power4_3.html - 42k - Cached - Similar pages

[PDF] Increasing Design Space of the **Instruction Queue** with Tag Coding
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4-issue instruction queue are shown in Figure 3. These simulation ... The **register rename** logic keeps track of the mapping from logic ...
www.egr.msu.edu/~mason/pubs/GLSVLSI2005-Zhou.pdf - Similar pages

[PDF] EE382A Lecture 8: Data-flow or Dynamic Scheduling Announcements ...
File Format: PDF/Adobe Acrobat - View as HTML
Scheduler entry monitors result bus for **rename register** Tag(s). • Find out if source operand becomes ready. – When all operands ready, **issue instruction** ...
www.stanford.edu/class/ ee382a/handouts/L08-dynamic_4up.pdf - Similar pages

[PDF] Microsoft PowerPoint - 291-06-metaflow.ppt
File Format: PDF/Adobe Acrobat - View as HTML
When all operands ready, **issue instruction** into Functional Unit ... Deferred-scheduling **Register-renaming Instruction** Shelf ...
www.lems.brown.edu/~iris/ en291s9-04/lectures/291-06-metaflow.pdf - Similar pages

[PDF] **Instruction Instruction** - - Level Parallelism and Level ...
File Format: PDF/Adobe Acrobat
... result Execution complete Read Operand **Issue Instruction** ... read or write for an earlier **instruction**. ... Dynamic Scheduling with **Register Renaming** Dynamic Scheduling ...
www.sc.isc.tohoku.ac.jp/class/uhsipa2003/10142003.pdf - Supplemental Result - Similar pages

[PPT] Pipeline CPI
File Format: Microsoft Powerpoint - View as HTML
Track when operands for **instructions** are available; Do **register renaming** to ... from **instruction queue**; If reservation station available, **issue instruction** ...
www.cs.appstate.edu/~can/ classes/5483/slides/chap3.1-3.3.ppt - Similar pages

[PPT] Lecture 11
File Format: Microsoft Powerpoint - View as HTML
If reservation station and reorder buffer slot free, **issue instruction** & send operands ... Precise exceptions; Speculative execution; **Register renaming** ...
www.cs.unc.edu/~montek/teaching/ fall-04/lectures/lecture-14.ppt - Similar pages

[PPT] Lecture 13
File Format: Microsoft Powerpoint - View as HTML
If reservation station and reorder buffer slot free, **issue instruction** & send operands & reorder buffer no. ... **Register renaming**. Solution in three steps ...
www.cs.unc.edu/~montek/teaching/ fall-03/lectures/lecture-14.ppt - Similar pages

[PPT] CS152: Computer Architecture and Engineering
File Format: Microsoft Powerpoint - View as HTML
Support **Register renaming**. Renames all destination registers: ... If reservation station free (no structural hazard), **issue instruction** & operand values (if ...

www.ece.uvic.ca/~amirali/courses/2006.lecture10.ppt - Similar pages

[PPT] homepages.cae.wisc.edu/~mikko/552/ch6c.ppt
File Format: Microsoft Powerpoint - View as HTML
Fetch alignment. **Instruction** cache misses. **Register** data flow. **Register renaming**: RAW/WAR/WAW. Memory data flow. In-order stores: WAR/WAW. Store **queue**: RAW ...
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"issue instruction "rename register" " Search

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Web Results **1** - **10** of about **134** for **"rename register" "coupled" "instruction queue"** . (**0.75** seconds)

esp@cenet description view
To achieve maximum performance, **rename register** allocation for each issued instruction ... Processors 101 are **coupled** to system memory 250 and various other ...
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Cached - Similar pages

Cache Latency and Out of Order Execution
... stations (ie each reservation station contains a **rename register**). ... length, Number of entries in the **Instruction Queue**. ... **Coupled** with the ability to specify the ...
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Supplemental Result - Cached - Similar pages

EP1099157 Advanced european software patent - Processor configured ...
The map unit is **coupled** to receive a plurality of destination register numbers ... An instruction operation remains in **instruction queue** 36A-36B at least ...
gauss.ffii.org/PatentView/EP1099157 - 132k - Cached - Similar pages

POWER4 system microarchitecture
Filling the **instruction queue** in front of the decode, crack, ... **Rename register**: For each register that is renamed and set by an instruction in the group, ...
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0018-8646/2002/$5.00 (C) 2002 IBM POWER4 system microarchitecture ...
Register-renaming pools and other out-of-order resources **coupled** with the pipeline ... Filling the **instruction queue** in front of the decode, crack, ...
www.research.ibm.com/journal/rd/461/tendler.txt - 90k - Cached - Similar pages
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Cycle count replication in a simultaneous and redundantly threaded ...
In addition, SRT processor 100 may also be **coupled** to other SRT processors if ... The register update unit ("RUU") 130 provides an **instruction queue** for the ...
www.freepatentsonline.com/6854051.html - 64k - Cached - Similar pages

United States Patent Application: 0040172631
If more than one **instruction queue** is used, each **instruction queue** typically ... **Rename register** cache 7 thus provides high-speed working register storage. ...
appft1.uspto.gov/.../ 20040172631&RS=DN/20040172631 - 48k - Cached - Similar pages

[PS] RuDRA: A REACTIVE DISSIPATION REDUCING ARCHITECTURE A Thesis ...
File Format: Adobe PostScript - View as HTML
Secondly, the overall design was modified to consist of loosely **coupled** ... Dispatch **Rename Register**. Figure 4.1. Baseline conventional superscalar ...
www.nd.edu/~arodrig6/papers/rudra.ps - Similar pages

[PDF] Pipelined & Superscalar processors
File Format: PDF/Adobe Acrobat - View as HTML
A **rename register** is allocated at. decode stage and the rename. remains in force until commit ... **Instruction queue**. Completion unit. with reorder buffer ...
staff.science.uva.nl/~jesshope/ Downloads/2.pipeline-processors.pdf - Similar pages

[PDF] MPC7410 RISC Microprocessor Technical Summary ...
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instruction is in the BTIC, it is fetched into the **instruction queue** a cycle sooner ... Data

returned from the cache is held in a **rename register** until the ...
www.freescale.com/files/ 32bit/doc/prod_brief/MPC7410TS.pdf - Similar pages

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